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EXAMINER	
IWASHKO, LEV	

ART UNIT	PAPER NUMBER
2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/620,406	VARTTI ET AL.	
	Examiner	Art Unit	
	Lev I. Iwashko	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/1/2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendments to Claims 1-2, 16-17, 25, 28, and 30 have been acknowledged.

2. Claims 1-37 stand rejected.

Claim Rejections - 35 USC § 102

3. The following are quotations of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-14, 16-26, and 28-37 are rejected under U.S.C. 102(b) as being anticipated by MacDonald (US Patent 5,913,224).

Claim 1. (AMENDED) A memory system, comprising: *(Abstract, lines 1-2 – Discloses a computer system and memory)*

- a programmable storage device to store one or more indicators; *(Title – Declares that this invention is a programmable cache)*
- a cache; *(Title)*
- cache tag logic; and *(Column 8, line 31 – Discloses a tag logic)*
- a control circuit coupled to the storage device *(Column 5, lines 1-6 – Declare a cache management unit (a.k.a. control circuit) that is coupled to an L2 cache memory (a.k.a. storage device))*
- the cache, and to the cache tag logic, *(Column 5, lines 47-48 – State that the cache management unit includes an address tag and a state logic unit. Column 8, lines 28-31 – State that the L2 cache subsystem includes tag logic*
- the control circuit to receive data for possible retention in the cache and to determine, based on the state of the one or more indicators,

whether to update the cache tag logic to track the data. *(Column 5, lines 3-8 – State that the cache management unit directs data transfers in and out of the L2 cache, and orchestrates the transfer of data, address and control signals between local bus and system memory, and also includes a memory controller (a.k.a. indicator))*

Claim 2. (AMENDED) The memory system of Claim 1,

- and wherein the control circuit further includes circuits to determine, based on the one or more indicators, whether to store the data to the cache. *(Column 5, lines 54-57 – State that the cache management unit may contain circuits for reading, writing, updating, invalidating, copy-back, and flush operations)*

Claim 3. The memory system of Claim 2, wherein one of the indicators indicates the cache is not available for use. *(Column 4, lines 60-67 – State that the L2 cache is able to lock in specified contents so that the material cannot be overwritten. That means that it will be in a state where the cache is not available for use)*

Claim 4. The memory system of Claim 2, and further including:

- at least one requester coupled to the control circuit to request data from, and store data to, the cache; *(Column 5, lines 15-20 – State that there is information requested by the system memory for storing into the L2 cache)*
- a main memory to provide to the cache requested data that is not stored within the cache; and *(Figure 2, Numbers 300 and 220)*
- wherein the control circuit includes a circuit that may replace the data in the cache based on the state of the indicators. *(Column 5, lines 47-52 – State that there is a write-back circuit that replaces data within the L2 cache based on a certain state (based on the state logic circuit))*

Claim 5. The memory system of Claim 4, wherein the main memory provides data to the cache in response to a request that is any one of multiple request types, wherein at least one of the indicators identifies one or more of the

request types, and wherein the control circuit prevents the replacement of the data in the cache if the data was provided in response to any of the identified request types. *(Column 5, lines 47-58 – Explain how the data is provided to the cache. A request is made (Column 5, lines 15-16), and there is a control circuit that prevents replacement of data (Column 6, lines 4-23))*

Claim 6. The memory system of Claim 4, wherein the one or more request types includes a request type indicating the data will be modified by a requester. *(Column7, lines 16-19 – State that there is a translation from virtual to physical address upon request)*

Claim 7. The memory system of Claim 4, wherein at least one of the indicators identifies one or more of the at least one requester, and wherein the control circuit replaces the data in the cache if the data was returned from the main memory in response to a request issued by any of the identified requesters. *(Column 5, lines 47-52 – State that there is a write-back circuit that replaces data within the L2 cache based on a certain state (based on the state logic circuit)) (Column 2, lines 38-46 – State that there is a request for data and the data in the cache is replaced)*

Claim 8. The memory system of Claim 4, wherein the main memory provides data to the cache with a response that is any one of multiple response types, wherein at least one of the indicators identifies one or more of the response types, *(Column 6, lines 53-54 – State that there is real time code which is transferred from system memory to the cache memory. Also see Figure 3)*

- and wherein the control circuit replaces the data in the cache if the data is returned from the main memory with any of the identified response types. *(Column 2, lines 38-46 – State that there is a request for data and the data in the cache is replaced)*

Claim 9. The memory system of Claim 2, and further including at least one requester coupled to the control circuit to return data to the cache tag

logic, and wherein the control circuit determines whether to store the returned data to the cache based on the state of at least one of the indicators. *(Column 10, lines 9-17 – State that there is tag logic which is updated by memory interface with new data, and replacement logic uses an algorithm for storage to the cache)*

Claim 10. The memory system of Claim 9, wherein the at least one requester returns data to the cache tag logic during an operation that is any one of multiple operation types, *(Column 10, lines 15-17 – State that tag logic is updated and replaced with new data)*

wherein the indicators include an indicator to identify one or more of the operation types, and wherein the control circuit stores the returned data to the cache if the returned data is returned during any of the identified operation types. *(Column 10, lines 44-55 – State that the comparator indicated to replacement logic that it should be stored in data way 0, due to the fact that the cache miss operation has been detected)*

Claim 11. The memory system of Claim 10, wherein the control circuit is further adapted to store the returned data to the cache based, at least in part, on whether a cache hit occurred. *(Column 5, lines 50-53)*

Claim 12. The memory system of Claim 9, and further including a main memory coupled to the control circuit, *(Figure 1, Numbers 200 and 300 – Show how the System memory and L2 Cache Subsystem are coupled together, with the L2 Cache Subsystem housing the control circuit)*

- and wherein the control circuit is adapted to forward the returned data to the main memory based, at least in part, on the state of at least one of the indicators. *(Column 8, lines 6-8 – State that the TLB entries are updated and the code is copied into the system memory)*

Claim 13. The memory system of Claim 12, wherein memory coherency actions may be incomplete for the returned data or for associated data retained by the at least one requester or the cache, and further including a request tracking circuit coupled to the control circuit to prevent the returned data from

being forwarded to the main memory until all of the memory coherency actions have been completed for the returned data or for the associated data. *(Column 6, lines 24-42 – Describe how the real-time code is extracted from the L2 cache to the system memory when it is complete, in order to maintain coherency)*

Claim 14. The memory system of Claim 1, wherein the programmable storage device includes circuits to store microcode, and wherein the control circuit is controlled by the microcode. *(Column 6, lines 29-34 – State that there is real time code that is stored by the L2 cache memory, and there is a cache management unit that is controlled by the code)*

Claim 16. (AMENDED) A method of controlling a memory system *(Column 8, line 66)* having cache tags to record which data is stored within one or more associated caches and further having one or more programmable control indicators, comprising: *(Column 5, lines 47-52)(Column 5, lines 22-23 – State the following: "*Associated with each line of L2 cache memory 201 is address tag and state information (not specifically shown)")

a.) obtaining data; and *(Column 9, lines 2-3 – State that the memory interface retrieves the data)*

b.) determining whether to update the cache tags to record the data based on the state of one or more of the control indicators. *(Column 9, lines 4-6 – Claim that the data is stored in one of two ways which is determined by the replacement logic)*

Claim 17. (AMENDED) The method of Claim 16, further including determining whether to store the data in a predetermined one of the associated caches based on the state of one or more of the control indicators. *(Column 5, lines 21-59 – Disclose a cache management unit which stores data based on the state information which comes from the state logic circuit)*

Claim 18. The method of Claim 17, wherein the memory system includes a main memory coupled to the cache tags, and wherein the obtaining step includes: *(Column 9, lines 64-66 – State that there is an address provided*

to processor interface which is compared to the tags stored in the tag logic)

- providing a request for the data to the main memory; and *(Column 5, lines 15-17)*
- receiving the data from the main memory. *(Column 1, lines 22-24)*

Claim 19. The method of Claim 18, wherein the request is any one of multiple types, *(Column 1, lines 27-28 – State that there is a request to either read or write data)*

- wherein one of the control indicators identifies one or more of the multiple request types, and wherein at least one of the determining steps is performed based, at least in part, upon whether the request is any of the identified response types. *(Column 2 lines 41-43 – State that there is a cache controller which determines the request)*

Claim 20. The method of Claim 18, wherein the data is provided from the main memory with a response type that is any one of multiple response types, wherein one of the control indicators identifies one or more of the multiple response types, and wherein at least one of the determining steps is performed based, at least in part, upon whether the request is any of the identified response types. (*Column 7, lines 42-50 – State that the cache management unit directs the requested instruction to be supplied to the CPU from the cache, in response to a requested instruction)*

Claim 21. The method of Claim 18, wherein the memory system is coupled to at least one requester, wherein one of the control indicators identifies one or more of the at least one requester, and wherein at least one of the determining steps is performed based, at least in part, upon whether the request was initiated by any of the identified requesters. *(Column 5, lines 15-20 – State that there is information requested by the system memory for storing into the L2 cache)*

Claim 22. The method of Claim 17, wherein the memory system is coupled to at least one requester, and wherein step a.) includes obtaining the data from

any one of the at least one requester. *(Column 5, lines 26-33 – State that the cache is capable of storing data of various sizes)*

Claim 23. The method of Claim 22, wherein the data is obtained during an operation that is any of multiple operation types, wherein one of the control indicators identifies one or more of the operation types, and wherein at least one of the determining steps is based, at least in part, on whether the data is obtained during any of the identified operation types. *(Column 5, lines 26-47 – State that the cache is capable of storing data of various sizes. Also, there is reference to clean and dirty data which results from various different operations)*

Claim 24. The method of Claim 23, wherein at least one of the determining steps is based, at least in part, on whether a cache hit occurs. *(Column 9, line 54)*

Claim 25. (AMENDED) The method of Claim 22, wherein the memory system includes a main memory, and further including providing the data to the main memory instead of storing the data into the predetermined on of the associated caches. *(Column 6, lines 24-29 – State that the code is stored I the system memory, and not in the L2 cache)*

Claim 26. The method of Claim 25, wherein the data is associated with incomplete memory coherency actions, and further including preventing the data from being provided to the main memory until all incomplete memory coherency actions have been completed. *(Column 6, lines 24-42 – Describe how the real-time code is extracted from the L2 cache to the system memory when it is complete, in order to maintain coherency)*

Claim 28. (AMENDED) A memory system, comprising:

- main memory means for storing data; *(Figure 4, Number 410)*
- cache means for storing a subset of the data; and *(Figure 4, Number 440)*
- programmable storage means for storing control indicators to determine how the subset of the data is to be selected. *(Title – States*

that this is a programmable system)(Column 5, lines 6-7 – State that the lock bit can be set)

Claim 29. The memory system of Claim 28, wherein requests are issued to the main memory to retrieve data from the main memory, and wherein the programmable storage means includes means for selecting the subset of the data based, at least in part, on a type of request that was issued to retrieve the subset of the data from the main memory. *(Column 5, lines 47-58 – Explain how the data is provided to the cache from the system memory. A request is made (Column 5, lines 15-16).*

Claim 30. (AMENDED) The memory system of Claim 28, and further including one or more requester means for causing data to be retrieved from the main memory, and wherein the programmable storage means includes means for selecting the subset of the data based, at least in part, on the identity of one or more of the requester means that caused data to be retrieved from the main memory. *(Column 5, lines 47-58 – Explain how the data is provided to the cache from the system memory. A request is made (Column 5, lines 15-16).*

Claim 31. The memory system of Claim 28, wherein the main memory means includes means for returning a response type to the cache means with data, and wherein the programmable storage means includes means for selecting the subset of the data based, at least in part, on the response type. *(Column 7, lines 42-50 – State that the cache management unit directs the requested instruction to be supplied to the CPU from the cache, in response to a requested instruction)*

Claim 32. The memory system of Claim 28, and further including requester means for returning data to the cache means, and wherein the programmable storage means includes means for selecting whether data returned by the requester means will be stored to the cache means. *(Column 5, lines 26-33 – State that the cache is capable of storing data of various sizes)*

Claim 33. The memory system of Claim 32, wherein the requester means includes

means for returning data during any of multiple types of operations, and wherein the programmable storage means includes means for selecting whether returned data will be stored to the cache means based, at least in part, on the type of operation that resulted in return of the data. *(Column 5, lines 26-47 – State that the cache is capable of storing data of various sizes. Also, there is reference to clean and dirty data which results from various different operations)*

Claim 34. The memory system of Claim 32, wherein the programmable storage means includes means for selecting whether data returned by the requester means will be stored to the cache means based, at least in part, on whether a cache miss occurred to the cache means. *(Column 7, lines 24-29 – State that a read miss occurs, and the cache management unit writes the data to the L2 cache)*

Claim 35. The memory system of Claim 28, and further including mode switch means for modifying the state of one or more of the control indicators based on monitored conditions occurring within the memory system. *(Column 7, lines 51-56 – Due to desiring to unlock real time code, the state of the lock bit is changed)*

Claim 36. The memory system of Claim 28, and wherein the cache means includes cache tag means for tracking data that may be stored to the cache means, and wherein the programmable storage means includes means for determining whether to update the cache tag means to track data. *(Column 5, lines 24-27 – State that there is an address tag which shows cache storing capability)*

Claim 37. The memory system of Claim 36, wherein the programmable storage means includes means for enabling the tracking by the cache tag means of predetermined data that is not included in the subset of the data stored within the cache means. *(Figure 1, Numbers 320 and 350 – Show real-time and non-real-time code which is in the system memory, and this shows how there can be tracking of data that is not included in the subset*

of the data stored within the cache means, because the no-re-time code is not, while the real-time code is stored within the cache means)

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 15 and 27 are rejected under 35 U.S.C.103(a) as being unpatentable over MacDonald as applied to claims 1 and 16 above.

MacDonald teaches the limitations of claims 1 and 16 for the reasons above.

MacDonald's invention differs from the claimed invention in that there is no specific reference to the automatically re-programming the indicators.

MacDonald fails to teach claims 15 and 27, which respectively state "The method of Claim 1, and further including mode switch logic coupled to the programmable storage device to automatically re-program at least one of the indicators in response to monitored conditions occurring within the memory system" and "The method of Claim 16, and further comprising: c.) monitoring conditions within the memory system; and d.) automatically re-programming at least one of the control indicators based on one or more of the monitored conditions." However, MacDonald does state that "State that there is a write-back circuit that replaces data within the L2 cache based on a certain state (based on the state logic circuit)" (Column 5, lines 47-52). Therefore, stating that the above is done automatically does not change the purpose or functionality of the claimed invention. Therefore, it would have been obvious to one of ordinary

skill in the art to enable MacDonald's "Programmable Cache" to automate the re-programming in order to make the whole programming process faster and more user-friendly.

For further information, reference Venner, 262 F.2d 91, 95, 120 USPQ 193, 194 (CCPA 1958) (Appellant argued that claims to a permanent mold casting apparatus for molding trunk pistons were allowable over the prior art because the claimed invention combined "old permanent-mold structures together with a timer and solenoid which automatically actuates the known pressure valve system to release the inner core after a predetermined time has elapsed." The court held that broadly providing an automatic or mechanical means to replace a manual activity which accomplished the same result is not sufficient to distinguish over the prior art.).

Response to Arguments

6. With regards to Claim 1, the Applicant alleges that "There is no indication in MacDonald that the MacDonald cache tag logic of the embodiment of Figure 5 is used in the embodiment of Figure 2 and vice versa. In particular, the cache management unit of Figure 2 does not determine whether to update the cache tag logic of Figure 5 based on any programmable indicators." The Applicant also states "nothing in MacDonald describes an aspect wherein the MacDonald cache management unit uses programmable indicators to determine whether to update the MacDonald address tags." Furthermore, the Applicant states "nothing in MacDonald discusses any operation whereby the cache tags may, or may not, be updated to track data that has been presented to the cache management unit." Finally, the Applicant alleges that "this device does not teach Applicants' programmable indicators used to determine whether to update cache tags to track data that has been provided to the cache." However, MacDonald discloses the following: "Cache management unit 202 includes an address tag and state logic circuit circuit (not specifically

shown) that contains and manages the address tag and state information. A comparator circuit for determining whether a cache hit has occurred, and a snoop write-back circuit that controls the write back of dirty data within L2 cache memory 201. It will be appreciated by those skilled in the art that cache management unit 202 may contain additional conventional circuits to control well-known caching functions such as various read, write, update, invalidate, copy-back, and flush operations. Such circuitry may be implemented using a variety of configurations" (Column 5, lines 47-58). MacDonald further states "Page allocations and TLB entries in step 415 are updated and if the code copied into system memory is a real-time module, the real-time bit in the corresponding TLB entry is updated" (Column 8, lines 6-9). If something is updatable, that means that it is programmable. Therefore, the Applicant's argument is moot in view of the prior art.

7. Claim 2 remains rejected based on the grounds of the rejection of Claim 1.

8. With regards to Claim 3, the Applicant alleges that "nothing in MacDonald teaches or suggests indicators to indicate the cache is not available for use". However, MacDonald states the following: "These lines of cache containing real-time code ultimately must be locked to prevent replacement" (Column 7, lines 5-6). If the cache lines are locked and cannot be overwritten, then they are not available for use. Therefore, the Applicant's argument is moot in view of the prior art.

9. With regards to Claim 4, the Applicant alleges that there is no mention of writing "from memory to cache". However, MacDonald states "A cache management unit provides the real-time code to the cache memory from system memory" (Abstract, lines 2-4). Therefore, the Applicant's argument is moot in view of the prior art.

10. Claims 5 and 6 remain rejected based on the grounds of the rejection of Claim 1. However, the Applicant further questions the relevance of the address translation function. Claim 6 further remains rejected due to the fact that the address translation function is in fact a modification that is completed upon request from a user. Therefore, the Applicant's argument is moot in view of the prior art.

11. Claim 7 remains rejected based on the grounds of the rejection of Claim 4.

12. With regards to Claim 8, the Applicant alleges that it is not understood how the invention "relates in any way to the memory providing data with a response that is any one of multiple type". However, MacDonald states the following: "During a cache miss, memory interface 295 is controlled by replacement logic 287 to store data corresponding to the new address (i.e., the address for which there was a cache miss) in one of the data ways. Memory interface 295 retrieves the requested data from system memory over lines 296 and stores the data in one of the two data ways as determined by replacement logic 287 in accordance with the present invention" (Column 8, lines 66-67 and Column 9, lines 1-6). Therefore, the Applicant's argument is moot in view of the prior art.

13. Claim 9 remains rejected.

14. Claims 10-11 remain rejected based on the grounds of the rejection of Claim 1.

15. With regards to Claim 12, the Applicant alleges that the "passage has nothing to do with copying code from any requestor to main memory". However, MacDonald states that the "Page allocations and TLB entries in step 415 are updated and if the code copied into system memory is a real-time module, the real-time bit in the corresponding TLB entry is updated" (Column 8, lines 6-9). Therefore, the Applicant's argument is moot in view of the prior art.

16. With regards to Claim 13, the Applicant alleges that "it is not understood how this passage teaches a request tracking circuit to prevent the return of data to main memory before all memory coherency actions have been completed". However, as previously stated, MacDonald states in lines 24-42 of Column 6 that there is a process of coherency that takes place before the code is unlocked to be sent to the system memory. The control circuit acts as the request tracking circuit as well. Therefore, the Applicant's argument is moot in view of the prior art.

17. Claim 14 remains rejected based on the grounds of the rejection of Claim 1.

18. Claim 16 remains rejected based on the grounds of the rejection of Claim 1.

19. Claims 17-26 stand rejected, as they are dependent on rejected Claim 16.

20. Claim 28 remains rejected based on the grounds of the rejection of Claim 1.

21. Claims 29-37 stand rejected, as they are dependent on rejected Claim 28.

22. Claims 15 and 27 stand rejected as they depend on rejected Claims 1 and 16, and furthermore only automate a manual process.

Conclusion

23. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

24. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lev I. Iwashko whose telephone number is (571)272-1658. The examiner can normally be reached on 9 Hours Schedule), from 8-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lev Iwashko

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